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PATENT
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IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Romain DESPLATS et al. Conf. 5660

Application No. 09/831,525 Group 2133

Filed May 10, 2001 Examiner C. Britt

METHOD AND INSTALLATION FOR FAST FAULT LOCALIZATION IN AN INTEGRATED CIRCUIT

SUBMISSION OF DRAWINGS

Assistant Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 16, 2004

Sir:

In response to PTOL-37 mailed May 17, 2004, replace the drawings originally filed with the accompanying new drawings.

Respectfully submitted,

YOUNG & THOMPSON

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